**REMARKS**

Claims 1-26 are currently pending, of which claims 1, 9, and 18 are in independent form.

Claims 10 and 19 have been amended. These amendments are supported by the application as filed, e.g., at page 16, lines 3-9. No new matter has been added.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

**Regarding the Claim Rejections - 35 U.S.C. §112, First Paragraph**

Claims 1-26 are rejected under 35 U.S.C. §112, First Paragraph, allegedly "as failing to comply with the enablement requirement." With regard to these rejections, the Examiner has stated:

> The specification lacks enablement with respect to the claimed limitation "hot signal" recited in the independent claim 1, 10 and 17. Even though, the definition of a "hot signal" is well known in the art, which may imply an active or live signal while the main power is still on, in this case the specification fails to adequately describe the definition of the hot signal as applied to the claimed invention.
>
> Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. Process Control Corp. v. HydReclaim Corp.,

> 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). In this case, the term "hot signal" in the claims is used by the claims to mean "an encoded signal during test", while the accepted meaning is "an active or live signal while the main power is still on." The term is indefinite because the specification does not clearly redefine the term. Therefore, for purpose of examination, the "hot signal" is given a broad interpretation to mean an encoded signal generated from a unit under test, when power is still on.

Applicant respectfully traverses the above enablement rejection and offers the following comments in response. Base claims 1, 9, and 18 do not recite a "hot signal", as the Examiner asserts, but rather a "one-hot signal". The term one-hot signal has a meaning that is well understood by one of ordinary skill in the art of digital circuits, i.e., a set of signal lines of which no more than one signal should be active at a time. A search on Google for "one-hot signals", as well as for the complementary term "one-hot state machines", brings up numerous references, including, for example, the article "Testing Digital Circuits with Constraints", Ahmad Al-Yamani *et al.*, available at www.crc.stanford.edu/crc_papers/alyamaniDFT02.pdf. The use of this terminology at the time the current application was filed is demonstrated, for example, by the article "Designing State Machines for FPGAs", copyrighted in September, 1997 by Actel Corporation; available at http://www.actel.com/documents/State_Machine_AN.pdf.

One of ordinary skill in the art would understand that the meaning of a "one-hot signal" in the present application conforms to the known usage of this term and would therefore not confuse *N* one-hot signals with *N* hot signals.

For at least the reasons discussed above, Applicant respectfully requests that the pending §112, First Paragraph, rejections be withdrawn.

**Regarding the Claim Rejections - 35 U.S.C. §112, Second Paragraph**

Claims 10 and 19 are rejected under 35 U.S.C. §112, Second Paragraph, as allegedly indefinite for the feature "wherein the N one-hot signals are operable to be encoded on an observability bus coupled to a general purpose performance counter." In response, claims 10 and 19 have been amended appropriately.

**Regarding the Claim Rejections - 35 U.S.C. §102(b)**

Claims 1-26 stand rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,644,578 to Ohsawa, hereinafter the *Ohsawa* reference. In connection with these rejections, the Examiner has commented as follows with respect to base claims 1, 9, and 18:

Regarding Claims 1, 8, 9, 14, 16, 18, Ohsawa discloses an apparatus and method for a failure memory device for storing failure data in a failure memory in a form of compressed data and can use the data read out from the failure memory as a mask pattern for masking a logical comparison result, Fig. 3, comprising:

An OR logic block comprising a logical comparison circuit 15 having four exclusive-OR circuits and a (mask circuit 16) for selectively masking data output from the logical comparison circuit 15 with the mask pattern stored in the register block (failure memory 17), where mask circuit 16 generates an N-bit output (four bit data), as shown in Fig. 3.

A Multiplexer (MUX) block comprising an OR circuit 18 and a multiplexer 19 for selecting the "Ored" output, which is stored in the register block (failure memory 17).

Applicant respectfully traverses the outstanding rejections under §102(b) and offers the following discussion as support. As currently constituted, base claim 1 is directed to an embodiment of a coverage capture circuit for use with a general purpose performance counter connected to a bus carrying *N* one-hot signals. The circuitry contains, *inter alia*, an OR logic block for bit-wise ORing the *N* one-hot signals with an *N*-bit mask value stored in a register block, the OR logic block operating to generate an *N*-bit output, and a Multiplexer (MUX) block operating to select the *N*-bit output from the OR logic block under control of at least one control signal, wherein the *N*-bit output is operable to be stored

into the register block when selected by the MUX block. Base claims 9 (method claim) and 18 (system claim) recite features corresponding to the circuit features of base claim 1.

The *Ohsawa* reference is directed to a failure memory device for compressing and storing failure data of a memory under test. See Abstract. Referring to FIG. 3 of the *Ohsawa* reference,

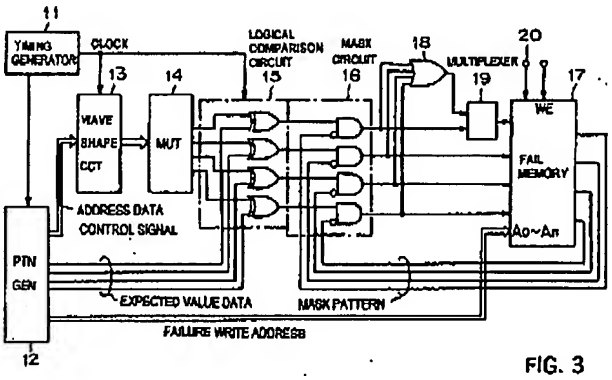


FIG. 3

logical comparison circuit 15 XORs the output from memory-under-test 14 with the data expected from the memory test to detect failed bits. Mask circuit 16 is used to mask the failure data so that the failure data cannot be written into the same address twice. The exemplary four signals output from the mask circuit are logically ORed by OR circuit 18; when bit compression is performed, the ORed output of circuit 18 is selected by multiplexer 19 and is inputted to the failure memory 17 instead of the output of one AND gate of mask circuit 16. See column 1, line 38 through column 2, line 8 and column 2, line 50 through column 3, line 5.

To the extent that the Examiner appears to equate the claimed OR logic block, mask, and multiplexer with the comparison circuit

15, mask circuit 16, and multiplexer 19 of *Ohsawa*, Applicant respectfully submits that it would be a mischaracterization to make such an identification.

Neither of the sets of signals received by logical comparison circuit 15 of *Ohsawa* are one-hot signals, as this term is understood by one of ordinary skill in the art. The first set of signals, received from memory-under-test 14, contains the results of the memory test; the values of these signals are dependent on the combination of specific signals sent to memory-under-test 14 and the condition of each cell of the memory, i.e., whether the cell is defective or not. Likewise, the second set of signals contains the expected results of the memory test, which is dependent again on the test performed. Neither of these sets of signals are constrained to be a one-hot signal. Nor do they anticipate or suggest the *N* one-hot signals as currently claimed.

Similarly, mask circuit 16 does not OR *N* one-hot signals with an N-bit mask. Besides the mask bits, the signals received in mask circuit 16 contains a record of any error detected; the value of these signals is determined by the presence or absence of defects in the memory under test.

Additionally, multiplexer 19 does not select an N-bit output from the OR logic block. As shown in Figure 3, multiplexer 19

selectively outputs either a single bit output from mask circuit 16 or else the ORed values of all of the values output from mask circuit 16.

Based on at least the foregoing analysis, it is believed that independent claim 1 is not anticipated or suggested by the *Ohsawa* reference and the rejection of claim 1 should therefore be withdrawn. Claims 9 and 18 contain features similar to those argued for claim 1; therefore the rejection of claims 9 and 18 should also be withdrawn. Claims 2-8 are dependent from base claim 1; claims 10-17 are dependent from base claim 9 and claims 19-26 are dependent from claim 18; each dependent claim introducing additional features in the respective base claims. Therefore, it is believed that the dependent claims are also in condition for allowance over the applied art.

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**SUMMARY AND CONCLUSION**

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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